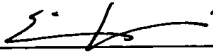


REMARKS

This amendment corrects minor typographical errors in the specification. Examination on the merits is requested.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE
IN THE SPECIFICATION:

Page 4, Paragraph 1

As an example of driving voltage applied during the light-emitting period, a voltage in a forward direction (forward bias voltage) is applied between the base layer [904] 903 and the emitter layer 905 such that the base layer [904] 903 and the collector layer 902 are set at an equal potential of 0 V.

Page 4, Paragraph 3 continuing on Page 5

During a light-extinct period, a voltage in a reverse direction (reverse bias voltage) is applied between the base layer 903 and the collector layer 902. This depletes substantially the entire region of the base layer [904] 903, as shown in the energy-band diagram of FIG. 19, so that the holes confined to the active layer 904 are extracted to the collector layer 902. If the holes can be extracted from the active layer 904 with sufficiently high efficiency, the concentration of the holes in the active layer 904 is reduced so that the quantity of carriers recombined for light emission is reduced and light emission is suppressed. Since the hole extracted operation is not dependent on the speed carrier recombination for light emission, light emission can be halted promptly so that high-speed modulation is allowed.

Page 40, Paragraph 2

In the [third] five embodiment, the impurity concentration in the base layer 504 has been adjusted to the about $1 \times 10^{17} \text{ cm}^{-3}$, while the impurity concentration in each of the collector layer 502 and the emitter layer 505 has been adjusted to $1 \times 10^{18} \text{ cm}^{-3}$.

Page 43, Paragraph 5 continuing on page 44

Although the fifth embodiment has used AlGaAs for the emitter layer [502] 505, if GaInP is used similarly to the collector layer 502, the effect of confining carriers to the base layer 504 can be enhanced. Conversely, if AlGaAs is used for the collector layer 502, the undoped semiconductor layer 503 or the graded composition layer can be formed between the base layer 504 and the collector layer 502 in an easier fabrication process.

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